



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,872	06/26/2003	John K. Walton	EMC2-143PUS	5270

45456 7590 12/04/2006

RICHARD M. SHARKANSKY  
PO BOX 557  
MASHPEE, MA 02649

EXAMINER
----------

CHEN, ALAN S

ART UNIT	PAPER NUMBER
----------	--------------

2182

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/606,872

Applicant(s)

WALTON ET AL.

Examiner

Alan S. Chen

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 and 18-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-13 and 19-21 is/are allowed.
- 6) ☒ Claim(s) 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 09/21/2006 pertaining to claims 12,13 and 19-21 have been fully considered and are persuasive. The prior art rejection of claims 12,13 and 19-21 is withdrawn.
2. Applicant's arguments filed 09/21/2006 pertaining to claim 18 has been fully considered but they are not persuasive. Applicant argues there is no electrical circuit in Locklear et al. and that Locklear et al. does not disclose inhibiting the electrical coupling of the electrical component one on PCB from electrical components of others.

Examiner points the Applicant to paragraph 25 of Locklear et al. As stated in the previous of Office Action, the Improvement Engine (*Fig. 1, element 112*) is the electrical circuit. Paragraph 25 expressly states the Improvement engine being a "programmable logic device or ASIC". Clearly, one of ordinary skill in the art views such elements as a 'circuit'. The purpose of the Improvement Engine is to optimize the data transfer between the PCBs and the I/O buses such that the best possible speed is utilized to make the system faster and more efficient. Fig. 2 shows various buses that the various PCBs can be operating on. During initialization, the Improvement Engine determines if a particular PCB is preventing the other PCBs on the bus from performing optimally, e.g., Fig. 2, element 116B is slower than the other PCBs and therefore being the bottleneck. The Improvement Engine tells the user to move the PCB element 116B to another slot element 108H. At this point, the PCB originally at element 116B is inhibited from communicating with 116A since they are not on the same bus anymore. Thus, as

Art Unit: 2182

stated in the previous office action, the Improvement Engine effectively inhibits the electrical coupling of the electrical component of one PCB to other PCBs. Paragraphs 25 through 33 explains discloses this in detail.

**Claim Rejections - 35 USC § 102**

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 18 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pat. Pub. No. 2002/0099875 to Locklear et al. (*Locklear*).

5. Per Claim 18, Locklear disclose method for operating a system (*Fig. 4 shows the method that is applied to Figs. 1 and 2, the system*), comprising: providing a backplane system (*Fig. 2, slots shown all intrinsically reside on a backplane*) comprising: a plurality of printed circuit boards (*Fig. 2, each slot holds a PCB*) each one having an electrical component thereon (*PCBs have electrical component, e.g., logic that performs some functionality; Paragraph 24 gives some examples such as RAID controllers, video adapters, graphic accelerators, etc*); and a backplane having plugged therein the plurality of printed circuit boards for producing a signal indicative of an operating incompatibility of the electrical components (*Fig. 2, elements 116x are signals that indicate an operating incompatibility. For instance, Fig. 2, element 116B flashes an*

Art Unit: 2182

*amber signal color to indicate the PCB, e.g., 66MHz, is not optimal for the slot, e.g., 100MHz; Paragraph 32); plugging an additional printed circuit board having an electrical component thereon into the provided backplane (Fig. 2, another PCB is plugged into empty slot 116D), the electrical component on such additional printed circuit board being incompatible with the speed of the electrical components on the plurality of printed circuit boards (Fig. 3, element 302; the PCB is operates at 66MHz, however it is plugged into a 100 MHz slot); an electrical circuit (Fig. 1, element 112, the improvement engine) for electrically inhibiting the electrical coupling the electrical component on the additional printed circuit board from the electrical components of the plurality of printed circuit boards (Fig. 4 shows that the PCBs are not allowed to communicate until optimization is completed. Furthermore, the improvement engine causes PCBs that slow down the bus to be removed from bus, inhibiting the communication with other PCBs on the bus).*

***Allowable Subject Matter***

6. Claims 1-11 are allowed based on previously stated reasons for allowance.
7. Claims 12, 13 and 19-21 are allowed.

The following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, ***all*** the limitations of the independent claim(s) (*claims 12 and 19*), particularly a plurality of PCBs plugged into the backplane, each PCB having a plurality of electrical contacts each contact indicating an operating incompatibility of an electrical component, wherein each one of the electrical contacts

Art Unit: 2182

are electrically connected through a corresponding one of a plurality of conductors of the backplane. US Pat. No. 6484222 to Olson et al. shows a plurality of conductors of a backplane that carry operating incompatibility signals of PCBs such that the signals from the conductors all feed to a controller (Fig. 2, element 100). However, Olson et al. does not teach or suggest, alone or in combination that the plurality of conductors are electrically connected together at the controller.

### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

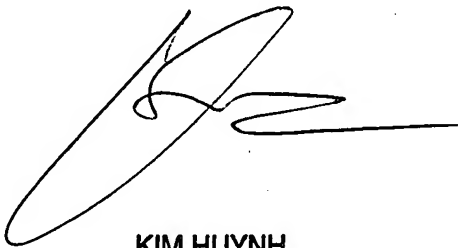
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

Art Unit: 2182

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC  
11/22/2006



KIM HUYNH  
SUPERVISORY PATENT EXAMINER

11/22/06